Computer Architecture HW 01

4th Edition Exercise 1.3.4-6

For problems below, use the information in the following table.

Processor	Clock rate	No. instructions	Time
P1	2 GHz	20×10^9	7 s
P2	1.5 GHz	30×10^9	10 s
P3	3 GHz	90×10^9	9 s

1.3.4 Find the IPC (instruction per cycle) for each processor.

1.3.5 Find the clock rate for P2 that reduces its execution time to that of P1.

1.3.6 Find the number of instructions for P2 that reduces its execution time to that of P3.

4th Edition Exercise 1.5.4-6

The table below shows instruction-type breakdown for different programs. Using this data, you will be exploring the performance tradeoffs with different changes made to a MIPS processor.

		# Instructions				
		Compute	Load	Store	Branch	Total
a.	Program 1	1000	400	100	50	1550
b.	Program 4	1500	300	100	100	2000

1.5.4 Assuming that computes take 1 cycle, loads and store instructions take 10 cycles, and branches take 3 cycles, find the execution time of each program on a 3 GHz MIPS processor.

1.5.5 Assuming that computes take 1 cycle, loads and store instructions take 2 cycles, and branches take 3 cycles, find the execution time of each program on a 3 GHz MIPS processor.

1.5.6 Assuming that computes take 1 cycle, loads and store instructions take 2 cycles, and branches take 3 cycles, what is the speed-up of a program if the number of compute instruction can be reduced by one-half?

4th Edition Exercise 1.7.1-3

The following table shows the increase in clock rate and power of eight generations of Intel processors over 28 years.

Processor	Clock rate	Power
80286 (1982)	12.5 MHz	3.3 W
80386 (1985)	16 MHz	4.1 W
80486 (1989)	25 MHz	4.9 W
Pentium (1993)	66 MHz	10.1 W
Pentium Pro (1997)	200 MHz	29.1 W
Pentium 4 Willamette (2001)	2 GHz	75.3 W
Pentium 4 Prescott (2004)	3.6 GHz	103 W
Core 2 Ketsfield (2007)	2.667 GHz	95 W

1.7.1 What is the geometric mean of the ratios between consecutive generations for both clock rate and power? (The geometric mean is described in Section 1.7.)

1.7.2 What is the largest relative change in clock rate and power between generations?

1.7.3 How much larger is the clock rate and power of the last generation with respect to the first generation?

4th Edition Exercise 1.12.1-3

The following table shows results for SPEC2006 benchmark programs running on an AMD Barcelona.

	Name	Intr. Count x 10^9	Execution Time (seconds)	Reference time (seconds)
a.	perl	2118	500	9770
b.	mcf	336	1200	9120

1.12.1 Find the CPI if the clock cycle time is 0.333 ns.

1.12.2 Find the SPEC ratio.

1.12.3 For these two benchmarks, find the geometric mean.

3rd Edition Exercise 4.10

Consider two different implementations, I1 and I2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. I1 has a clock rate of 6 GHz, and I2 has a clock rate of 3 GHz. The average number of cycles for each instruction class on I1 and I2 is given in the following table:

Class	CPI on I1	CPI on I2	C1 Usage	C2 Usage	C3 Usage
A	2	1	40%	40%	50%
B	3	2	40%	20%	25%
C	5	2	20%	40%	25%

The table also contains a summary of average proportion of instruction classes generated by three different compilers. C1 is a compiler produced by the makers of I1, C2 is produced by the makers of I2, and the other compiler is a third-party product. Assume that each compiler uses the same number of instructions for a given program but that the instruction mix is as described in the table.

Q. Using C1 on both I1 and I2, how much faster can the makers of I1 claim I1 is compared to I2?
Q. Using C2, how much faster can the makers of I2 claim that I2 is compared to I1?
Q. If you purchased I1, which compiler would you use?
Q. If you purchased I2, which compiler would you use?
Q. Which computer and compiler would you purchase if all other criteria were identical, including cost?