

# Arithmetic Circuits

Prof. Taewhan Kim  
(tkim@ssl.snu.ac.kr)

## Sources:

1. I. Koren, "Computer Arithmetic Algorithms," Natick, Massachusetts, 2001.
2. R. Katz, "Contemporary Logic Design," Prentice Hall, 2004.

# Contents

- Number system
- Addition/subtraction
  - Ripple-carry-adder
  - Carry-lookahead-adder
  - Carry-select-adder
- ALU
- Multiplication
  - Sequential multiplication
  - Fast multiplication
    - Partial products reduction techniques
    - Constant multiplication
- Division (not covered)
- Floating point (not covered)

# Number systems

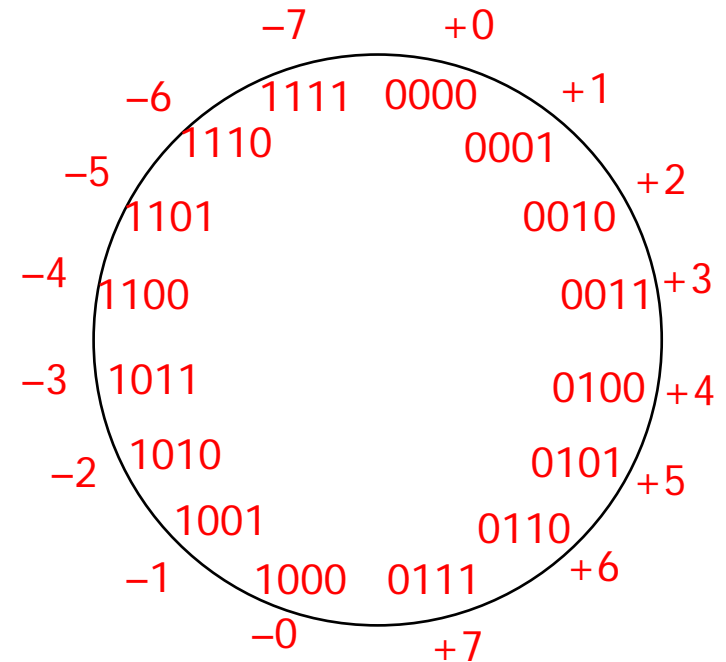
- Representation of positive numbers is the same in most systems
- Major differences are in how negative numbers are represented
- Representation of negative numbers come in three major schemes
  - sign and magnitude
  - 1s complement
  - 2s complement
- Assumptions
  - we'll assume a 4 bit machine word
  - 16 different values can be represented
  - roughly half are positive, half are negative

# Sign and magnitude

- One bit dedicate to sign (positive or negative)
  - sign: 0 = positive (or zero), 1 = negative
- Rest represent the absolute value or magnitude
  - three low order bits: 0 (000) thru 7 (111)
- Range for n bits
  - $\pm(2^{n-1} - 1)$  (two representations for 0)
- Cumbersome addition/subtraction
  - must compare magnitudes to determine sign of result

$$0\ 100 = +4$$

$$1\ 100 = -4$$



# 1s complement

- If  $N$  is a positive number, then the negative of  $N$  (its 1s complement or  $N'$ ) is  $N' = (2^n - 1) - N$ 
  - example: 1s complement of 7

$$\begin{array}{rcl} 2^4 & = & 10000 \\ 1 & = & 00001 \\ \hline 2^4 - 1 & = & 1111 \\ 7 & = & 0111 \\ \hline & & 1000 = -7 \text{ in 1s complement form} \end{array}$$

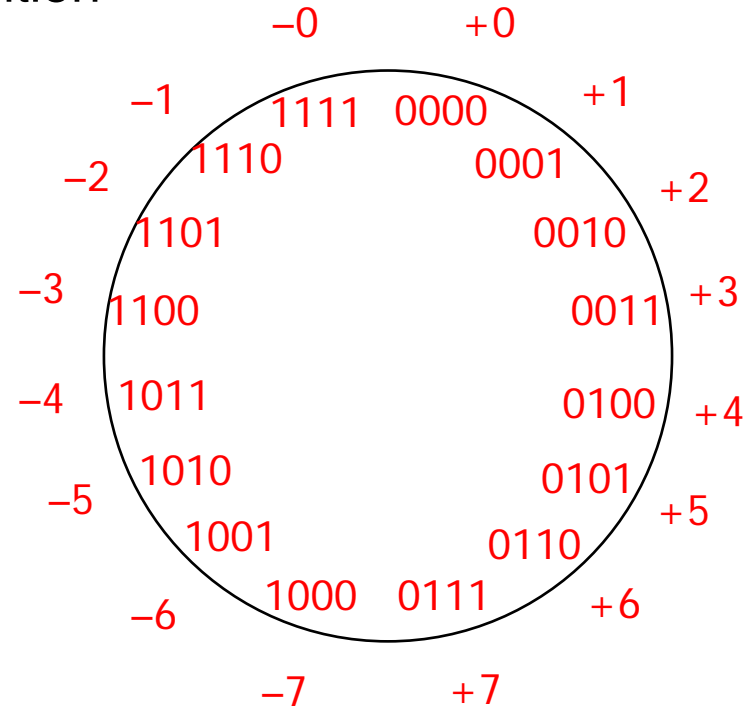
- shortcut: simply compute bit-wise complement ( 0111 -> 1000 )

# 1s complement (cont'd)

- Subtraction implemented by 1s complement and then addition
- Two representations of 0
  - causes some complexities in addition
- High-order bit can act as sign bit

$$0\ 100 = +4$$

$$1\ 011 = -4$$

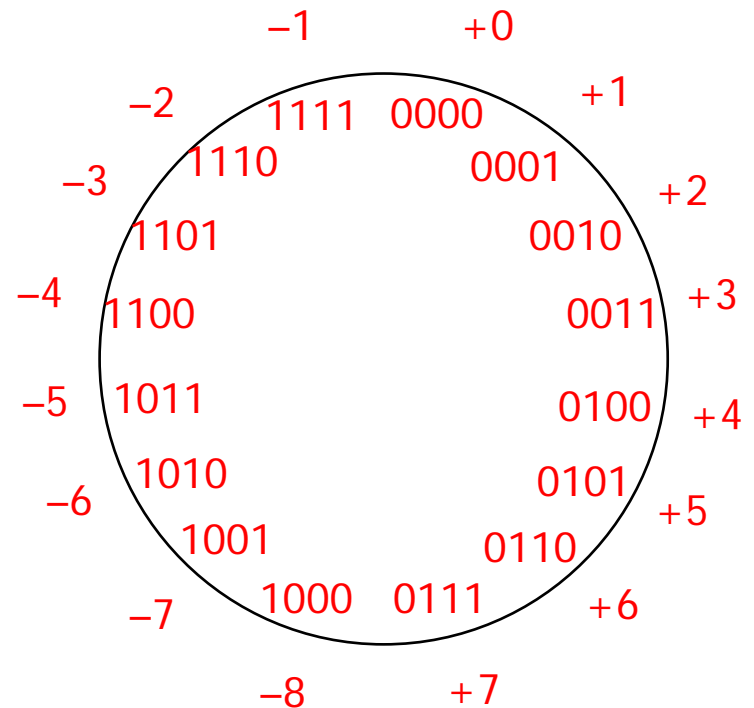


# 2s complement

- 1s complement with negative numbers shifted one position clockwise
  - only one representation for 0
  - one more negative number than positive numbers
  - high-order bit can act as sign bit

$$0\ 100 = +4$$

$$1\ 100 = -4$$



# 2s complement (cont'd)

- If N is a positive number, then the negative of N (its 2s complement or  $N^*$ ) is  $N^* = 2^n - N$

- example: 2s complement of 7

$$\begin{array}{r} 2^4 = 10000 \\ \text{subtract } 7 = \underline{0111} \\ 1001 = \text{repr. of } -7 \end{array}$$

- example: 2s complement of  $-7$

$$\begin{array}{r} 2^4 = 10000 \\ \text{subtract } -7 = \underline{1001} \\ 0111 = \text{repr. of } 7 \end{array}$$

- shortcut: 2s complement = bit-wise complement + 1
  - 0111  $\rightarrow$  1000 + 1  $\rightarrow$  1001 (representation of -7)
  - 1001  $\rightarrow$  0110 + 1  $\rightarrow$  0111 (representation of 7)



# 2s complement addition and subtraction

- Simple addition and subtraction
  - simple scheme makes 2s complement the virtually unanimous choice for integer number systems in computers

$$\begin{array}{r} 4 \quad 0100 \\ + 3 \quad 0011 \\ \hline 7 \quad 0111 \end{array} \qquad \begin{array}{r} -4 \quad 1100 \\ + (-3) \quad 1101 \\ \hline -7 \quad 11001 \end{array}$$

$$\begin{array}{r} 4 \quad 0100 \\ - 3 \quad 1101 \\ \hline 1 \quad 10001 \end{array} \qquad \begin{array}{r} -4 \quad 1100 \\ + 3 \quad 0011 \\ \hline -1 \quad 1111 \end{array}$$

# Why can the carry-out be ignored?

- Can't ignore it completely
  - needed to check for overflow (see next two slides)
- When there is no overflow, carry-out may be true but can be ignored

–  $M + N$  when  $N > M$ :

$$M^* + N = (2^n - M) + N = 2^n + (N - M)$$

ignoring carry-out is just like subtracting  $2^n$

–  $M + -N$  where  $N + M \leq 2^{n-1}$

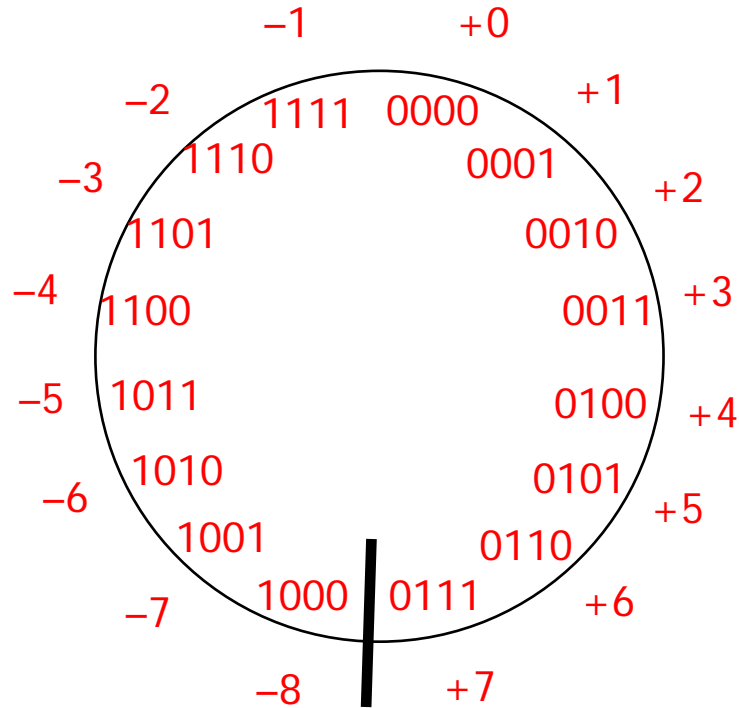
$$(-M) + (-N) = M^* + N^* = (2^n - M) + (2^n - N) = 2^n - (M + N) + 2^n$$

ignoring the carry, it is just the 2s complement representation for  $-(M + N)$

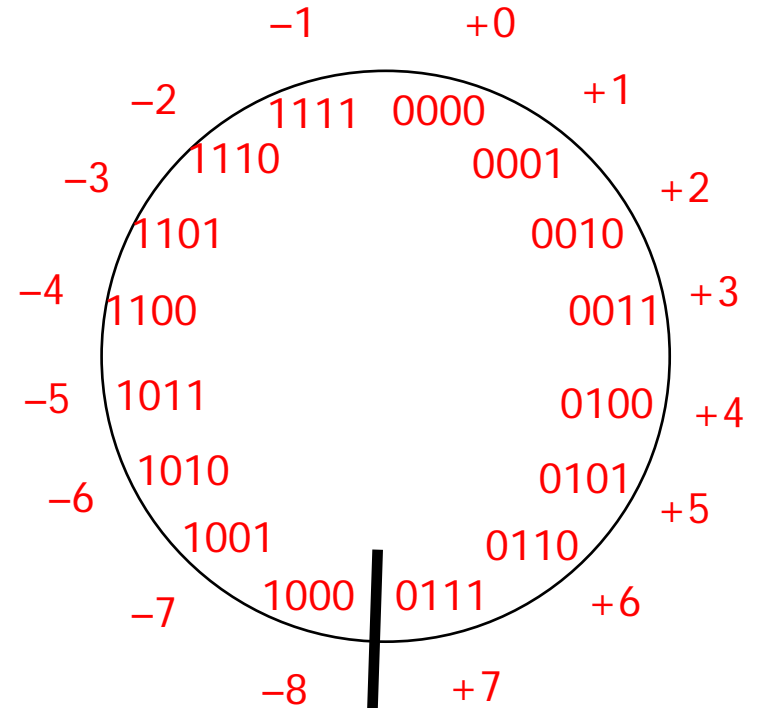
# Overflow in 2s complement addition/subtraction

- Overflow conditions

- add two positive numbers to get a negative number
- add two negative numbers to get a positive number



$5 + 3 = -8$



$-7 - 2 = +7$

# Overflow conditions

- Overflow when carry into sign bit position is not equal to carry-out

$$\begin{array}{r}
 5 \\
 \underline{-3} \\
 -8
 \end{array}
 \quad
 \begin{array}{r}
 0111 \\
 0101 \\
 \underline{0011} \\
 1000
 \end{array}$$

overflow

$$\begin{array}{r}
 -7 \\
 \underline{-2} \\
 7
 \end{array}
 \quad
 \begin{array}{r}
 1000 \\
 1001 \\
 \underline{1110} \\
 10111
 \end{array}$$

overflow

$$\begin{array}{r}
 5 \\
 \underline{2} \\
 7
 \end{array}
 \quad
 \begin{array}{r}
 0000 \\
 0101 \\
 \underline{0010} \\
 0111
 \end{array}$$

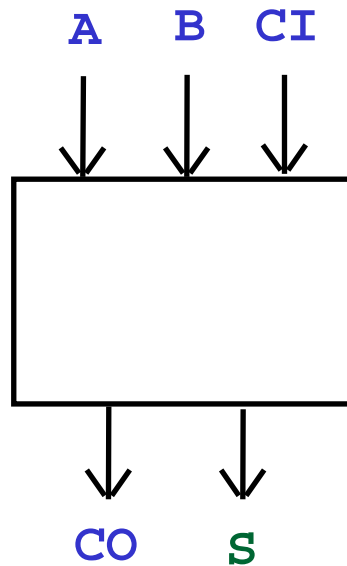
no overflow

$$\begin{array}{r}
 -3 \\
 \underline{-5} \\
 -8
 \end{array}
 \quad
 \begin{array}{r}
 1111 \\
 1101 \\
 \underline{1011} \\
 11000
 \end{array}$$

no overflow

# Addition: binary addition

- This is the primitive of almost all arithmetic computation.



Truth Table:

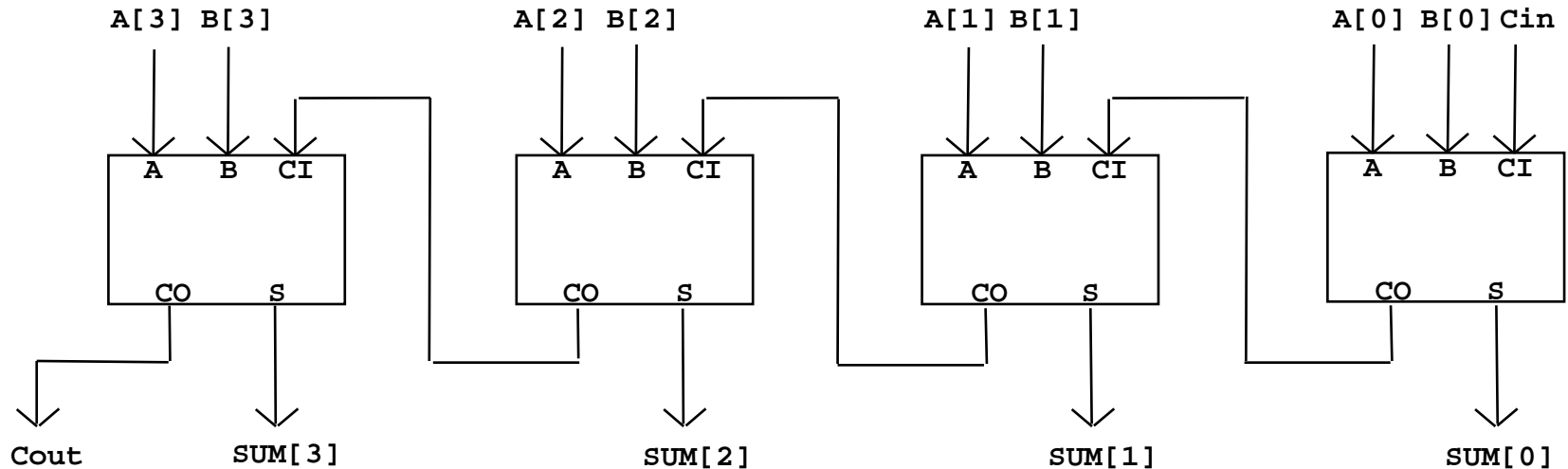
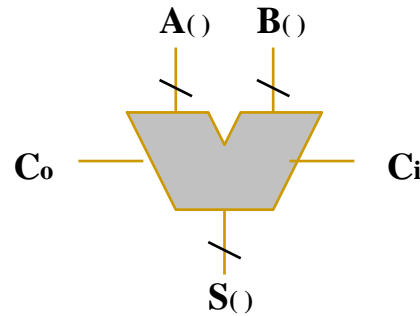
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$CO = A \cdot B + B \cdot CI + CI \cdot A$$

$$S = A \oplus B \oplus CI$$

# A 4-Bit Ripple-Carry Adder (RCA)

- Note: The carry chain ripples from the least to the most significant bit (LSB to MSB).

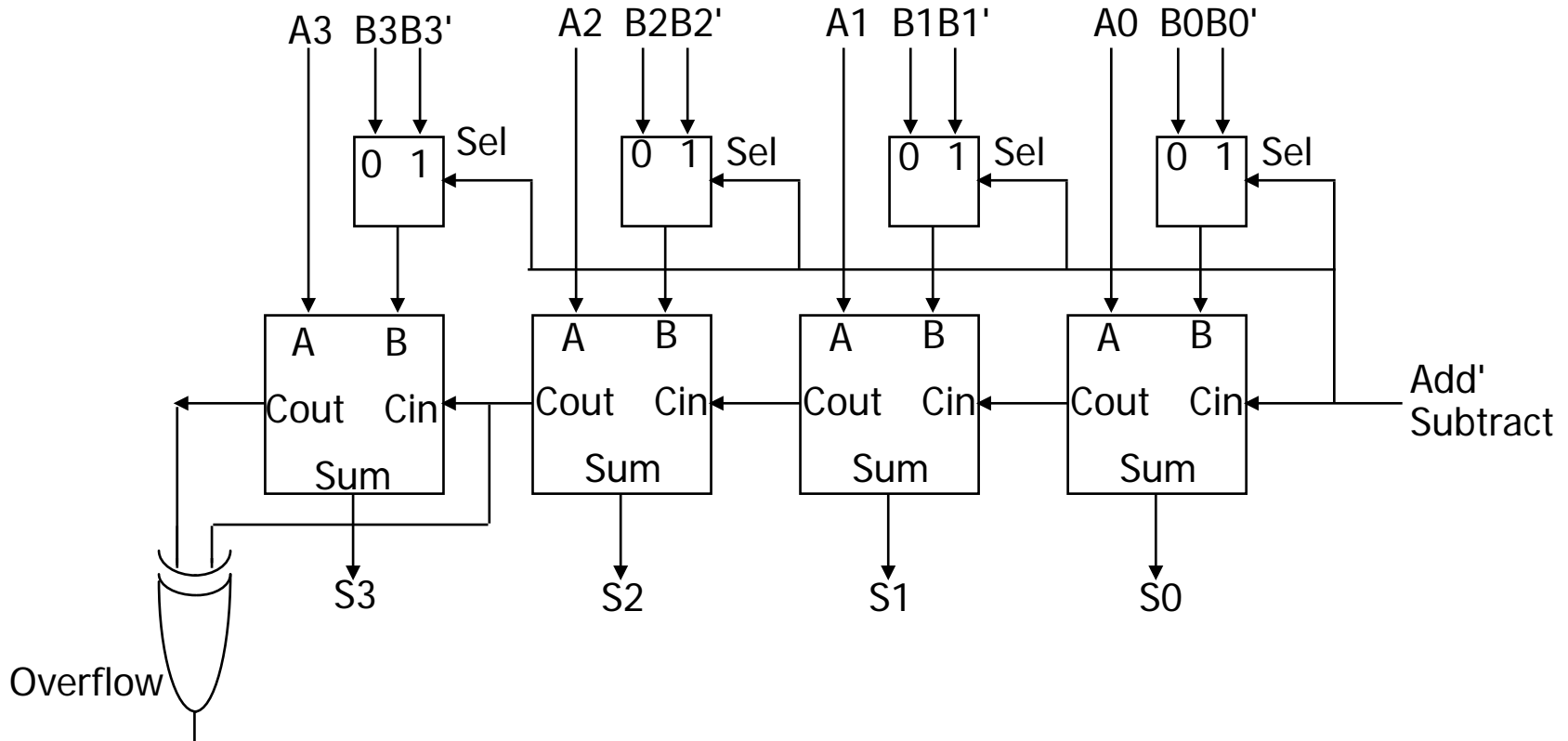


Area = (bit-width) \* (area of a one-bit full-adder cell)

Delay = (bit-width) \* (delay of a one-bit full-adder cell)

# Adder/subtractor

- Use an adder to do subtraction thanks to 2s complement representation
  - $A - B = A + (-B) = A + B' + 1$
  - control signal selects B or 2s complement of B



# Carry-lookahead logic

- Carry generate:  $G_i = A_i B_i$ 
  - must generate carry when  $A = B = 1$
- Carry propagate:  $P_i = A_i \text{ xor } B_i$ 
  - carry-in will equal carry-out here
- Sum and Cout can be re-expressed in terms of generate/propagate:
  - $S_i = A_i \text{ xor } B_i \text{ xor } C_i$   
 $= P_i \text{ xor } C_i$
  - $C_{i+1} = A_i B_i + A_i C_i + B_i C_i$   
 $= A_i B_i + C_i (A_i + B_i)$   
 $= A_i B_i + C_i (A_i \text{ xor } B_i)$   
 $= G_i + C_i P_i$

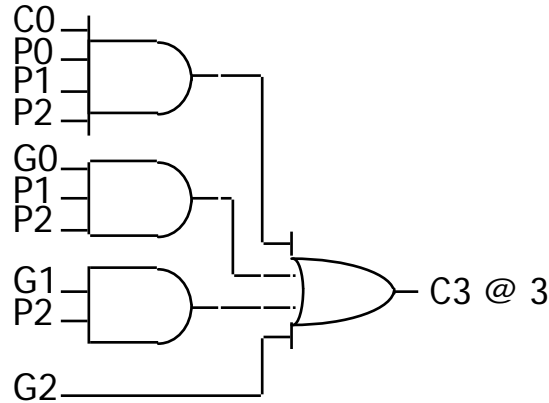
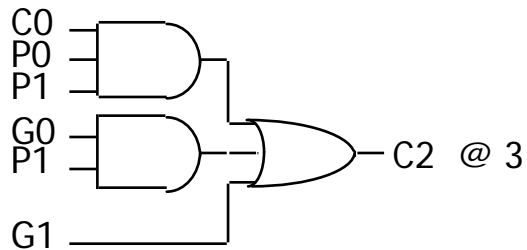
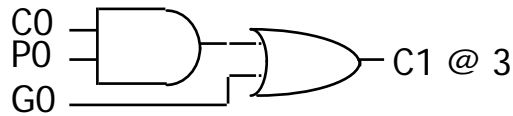
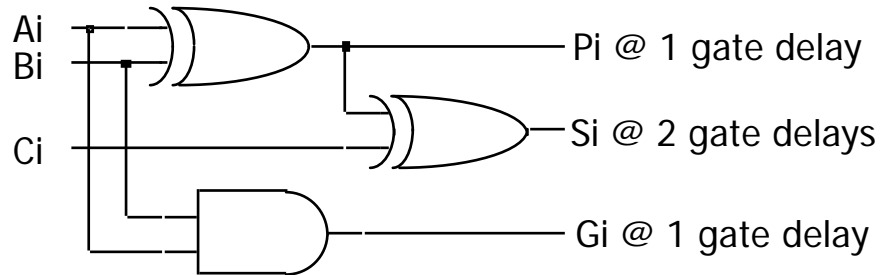


# Carry-lookahead logic (cont'd)

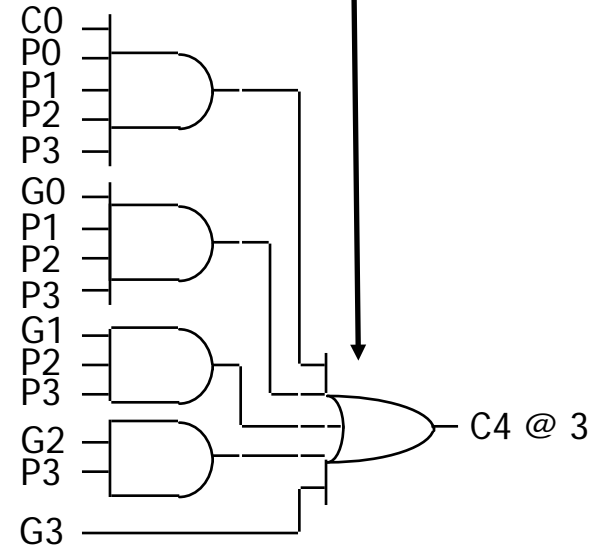
- Re-express the carry logic as follows:
  - $C_1 = G_0 + P_0 C_0$
  - $C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0 + P_1 P_0 C_0$
  - $C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$
  - $C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$
- Each of the carry equations can be implemented with two-level logic
  - all inputs are now directly derived from data inputs and not from intermediate carries
  - this allows computation of all sum outputs to proceed in parallel

# Carry-lookahead implementation

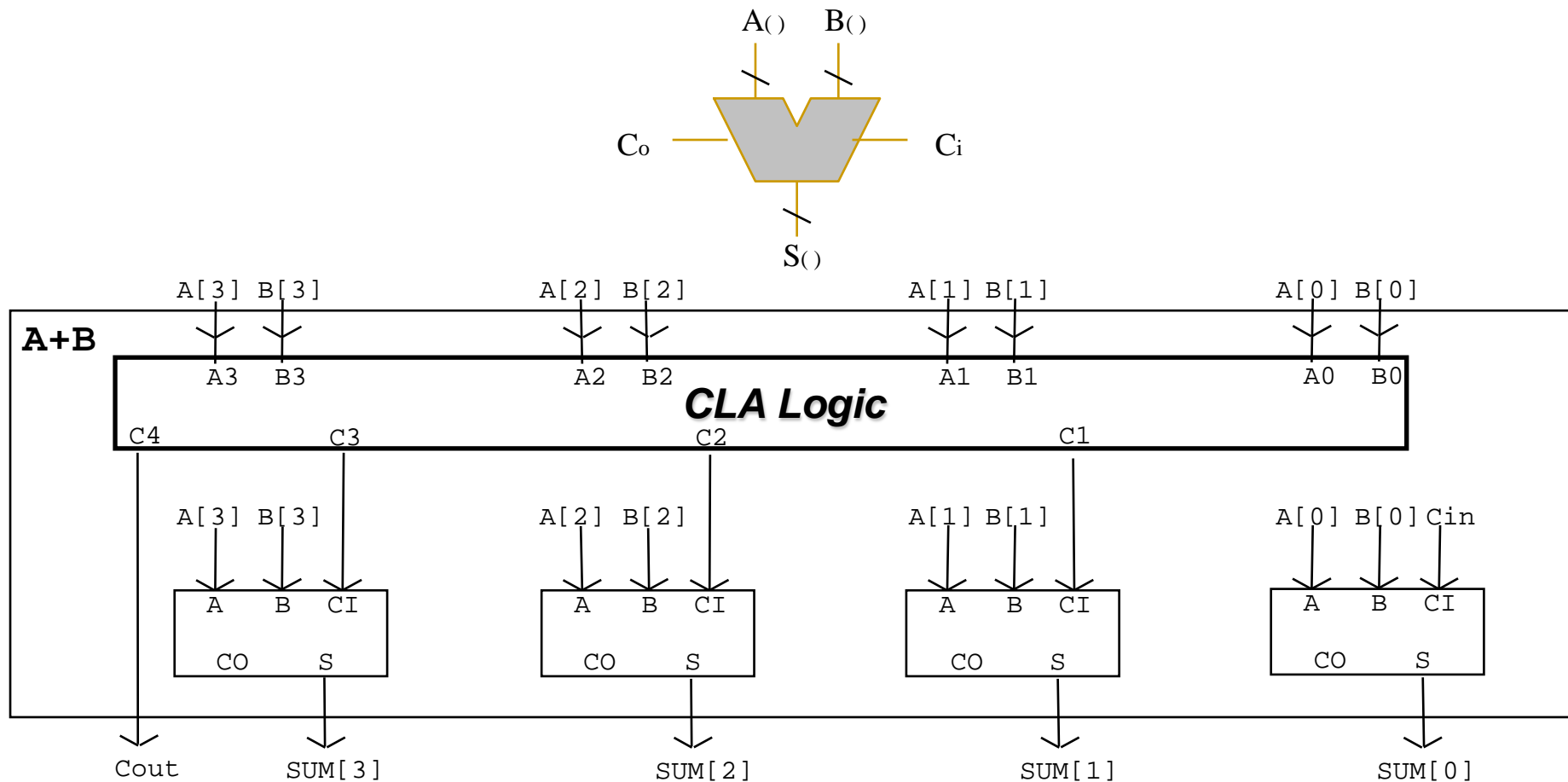
- Adder with propagate and generate outputs



increasingly complex  
logic for carries



# 4-Bit Carry Look Ahead (CLA) Adder

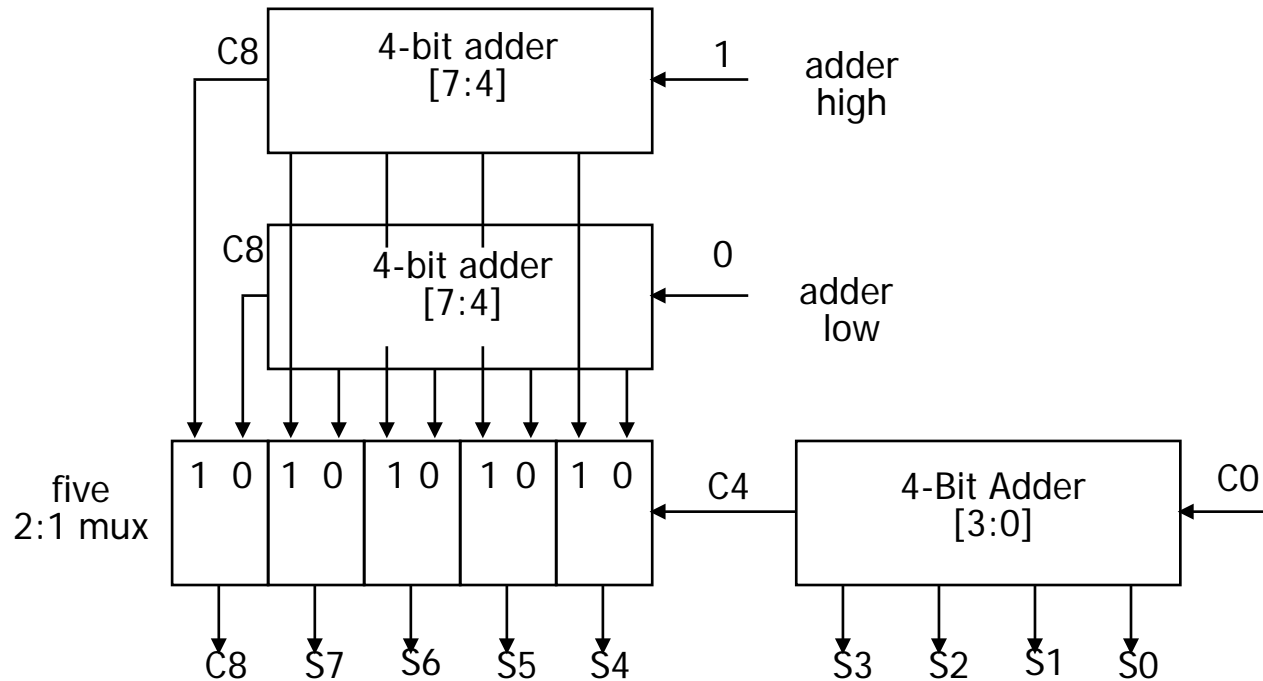


Area = (CLA Logic Area) + ((bit-width) \* (area of a one-bit full-adder cell))  
 = about  $(1 + \log_2(\text{bit-width}))$  \* (area of ripple adder)

Delay = about  $(1 + \log_2(\text{bit-width}))$  \* (delay of a one-bit full-adder cell)

# Carry-select adder

- Redundant hardware to make carry calculation go faster
  - compute two high-order sums in parallel while waiting for carry-in
  - one assuming carry-in is 0 and another assuming carry-in is 1
  - select correct result once carry-in is finally computed



# Arithmetic logic unit (ALU) design specification

**M = 0, logical bitwise operations**

S1	S0	Function	Comment
0	0	$F_i = A_i$	input $A_i$ transferred to output
0	1	$F_i = \text{not } A_i$	complement of $A_i$ transferred to output
1	0	$F_i = A_i \text{ xor } B_i$	compute XOR of $A_i, B_i$
1	1	$F_i = A_i \text{ xnor } B_i$	compute XNOR of $A_i, B_i$

**M = 1, C0 = 0, arithmetic operations**

0	0	$F = A$	input A passed to output
0	1	$F = \text{not } A$	complement of A passed to output
1	0	$F = A \text{ plus } B$	sum of A and B
1	1	$F = (\text{not } A) \text{ plus } B$	sum of B and complement of A

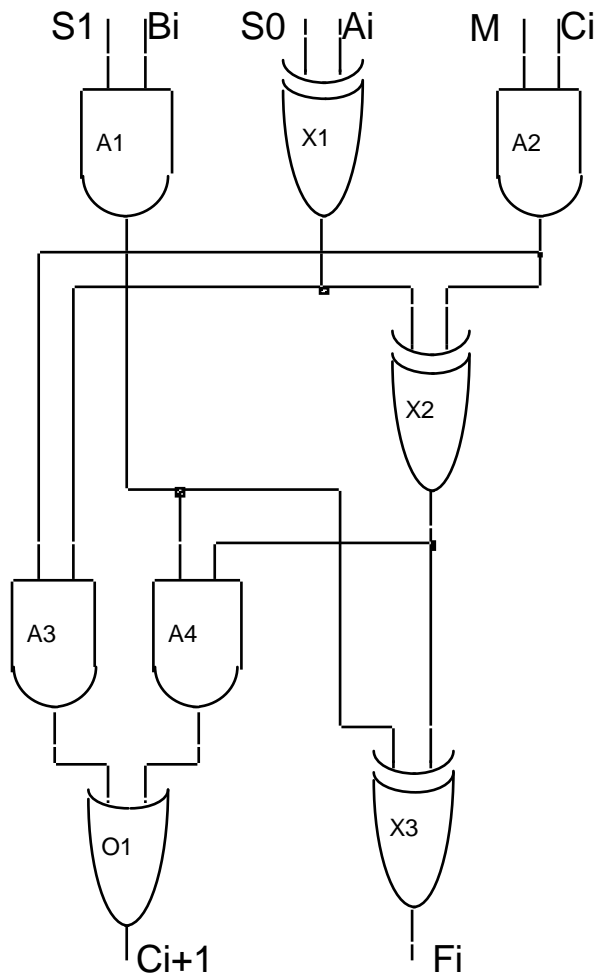
**M = 1, C0 = 1, arithmetic operations**

0	0	$F = A \text{ plus } 1$	increment A
0	1	$F = (\text{not } A) \text{ plus } 1$	twos complement of A
1	0	$F = A \text{ plus } B \text{ plus } 1$	increment sum of A and B
1	1	$F = (\text{not } A) \text{ plus } B \text{ plus } 1$	B minus A

logical and arithmetic operations  
not all operations appear useful, but "fall out" of internal logic

# ALU design

## ■ Sample ALU –multi-level implementation



first-level gates

use S0 to complement Ai

S0 = 0 causes gate X1 to pass Ai

S0 = 1 causes gate X1 to pass Ai'

use S1 to block Bi

S1 = 0 causes gate A1 to make Bi go forward as 0  
(don't want Bi for operations with just A)

S1 = 1 causes gate A1 to pass Bi

use M to block Ci

M = 0 causes gate A2 to make Ci go forward as 0  
(don't want Ci for logical operations)

M = 1 causes gate A2 to pass Ci

other gates

for M=0 (logical operations, Ci is ignored)

$$F_i = S_1 B_i \text{ xor } (S_0 \text{ xor } A_i)$$

$$= S_1' S_0' (A_i) + S_1' S_0 (A_i') +$$

$$S_1 S_0' (A_i B_i' + A_i' B_i) + S_1 S_0 (A_i' B_i' + A_i B_i)$$

for M=1 (arithmetic operations)

$$F_i = S_1 B_i \text{ xor } ((S_0 \text{ xor } A_i) \text{ xor } C_i) =$$

$$C_{i+1} = C_i (S_0 \text{ xor } A_i) + S_1 B_i ((S_0 \text{ xor } A_i) \text{ xor } C_i) =$$

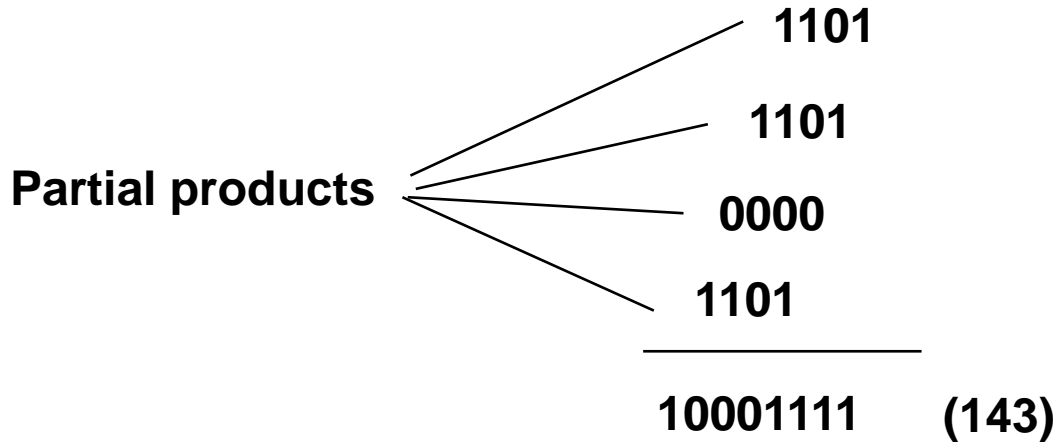
just a full adder with inputs S0 xor Ai, S1 Bi, and Ci

# Multiplication

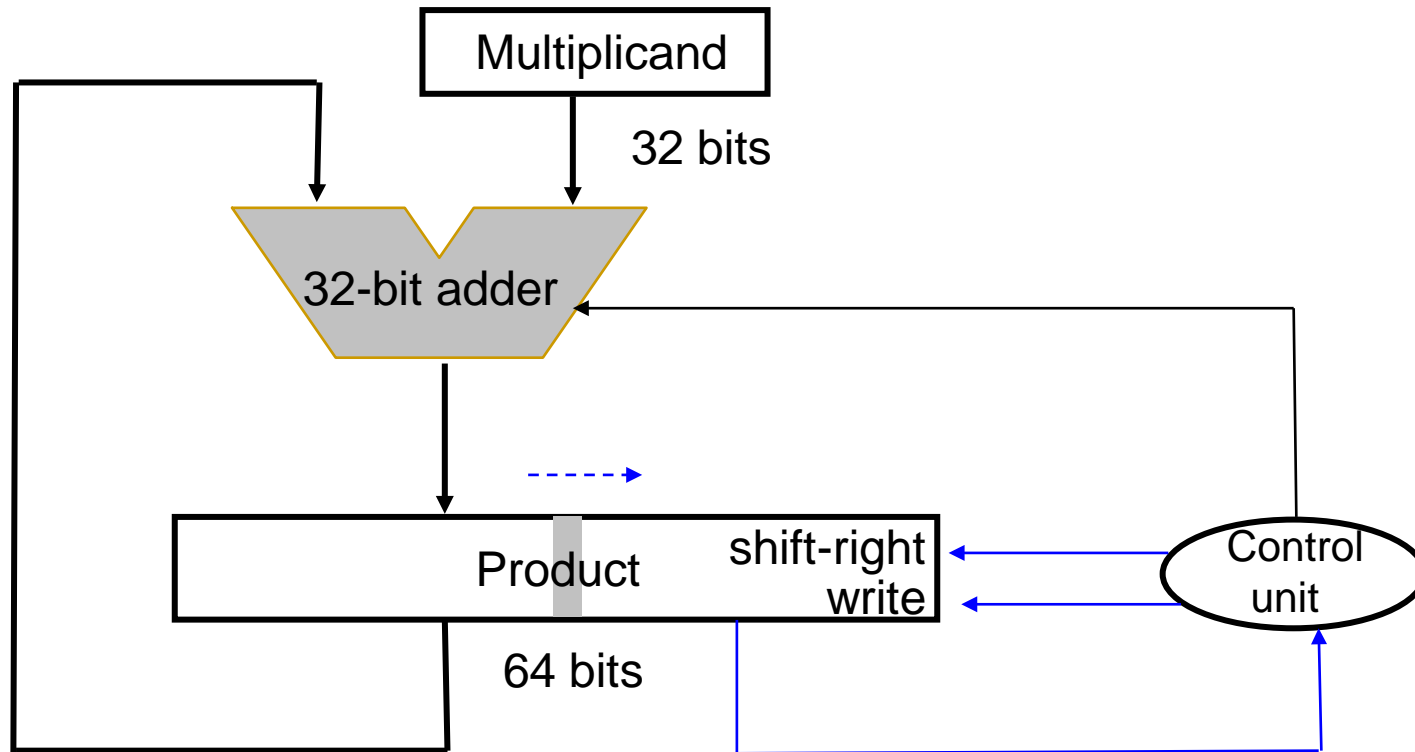
**multiplicand**            **1101 (13)**

**multiplier**            **\* 1011 (11)**

**product of 2 4-bit numbers  
is an 8-bit number**



# Sequential Multiplier



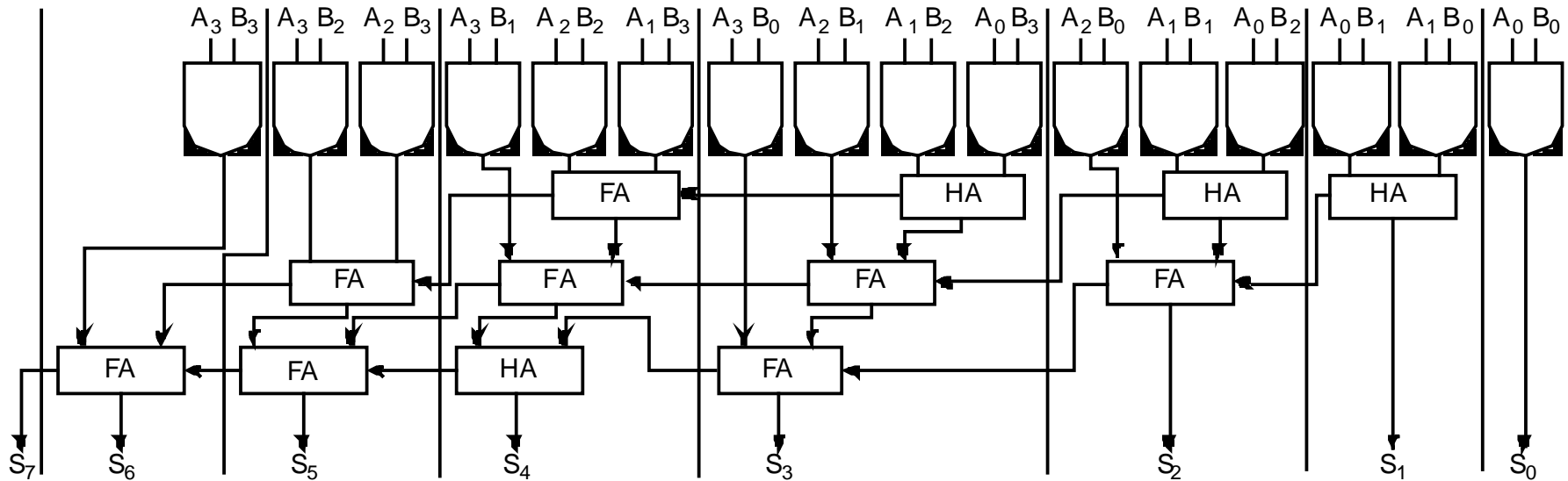


# Partition Products

*Partial Product Accumulation*

				A3	A2	A1	A0
				B3	B2	B1	B0
				A2 B0	A2 B0	A1 B0	A0 B0
			A3 B1	A2 B1	A1 B1	A0 B1	
		A3 B2	A2 B2	A1 B2	A0 B2		
A3 B3	A2 B3	A1 B3	A0 B3				
S7	S6	S5	S4	S3	S2	S1	S0

# Reduction Example



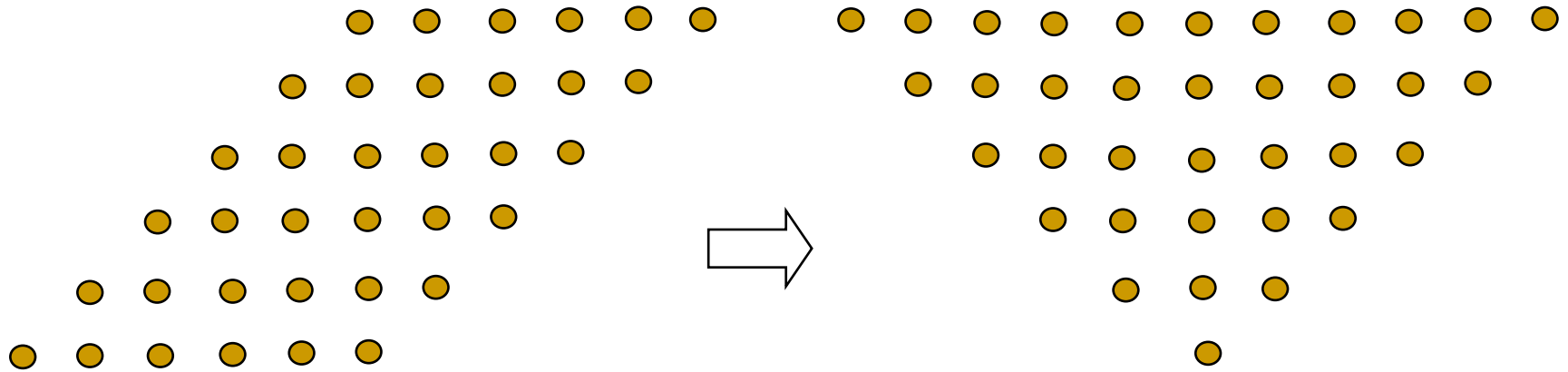
**Note use of parallel carry-outs to form higher order sums**

**12 Adders, if full adders, this is 6 gates each = 72 gates**

**16 gates form the partial products**

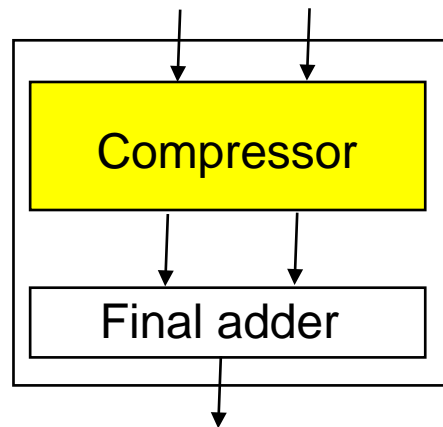
**total = 88 gates!**

# Example: Six partial products to be added



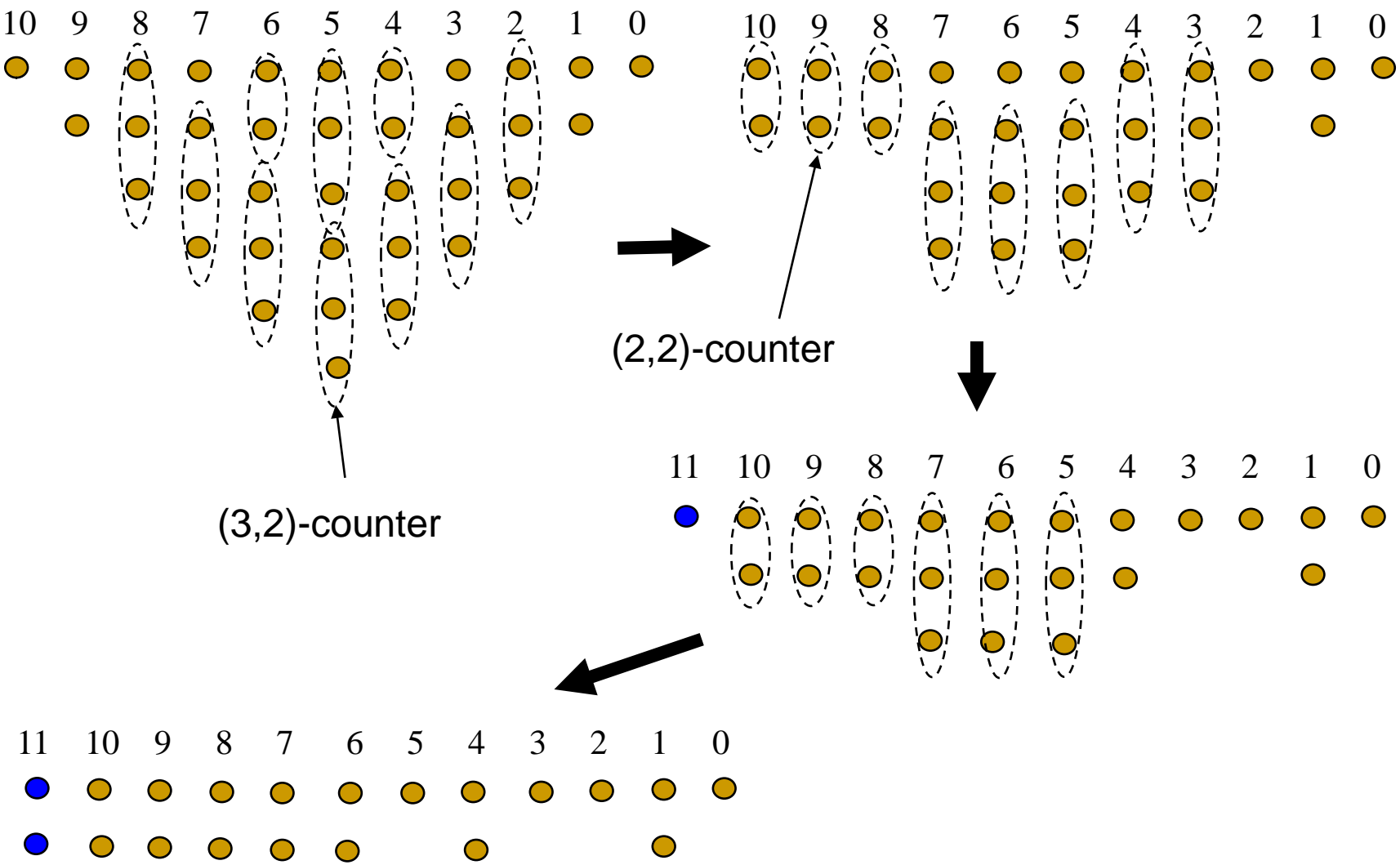
Original matrix of 36-bits

Reorganized matrix of bits

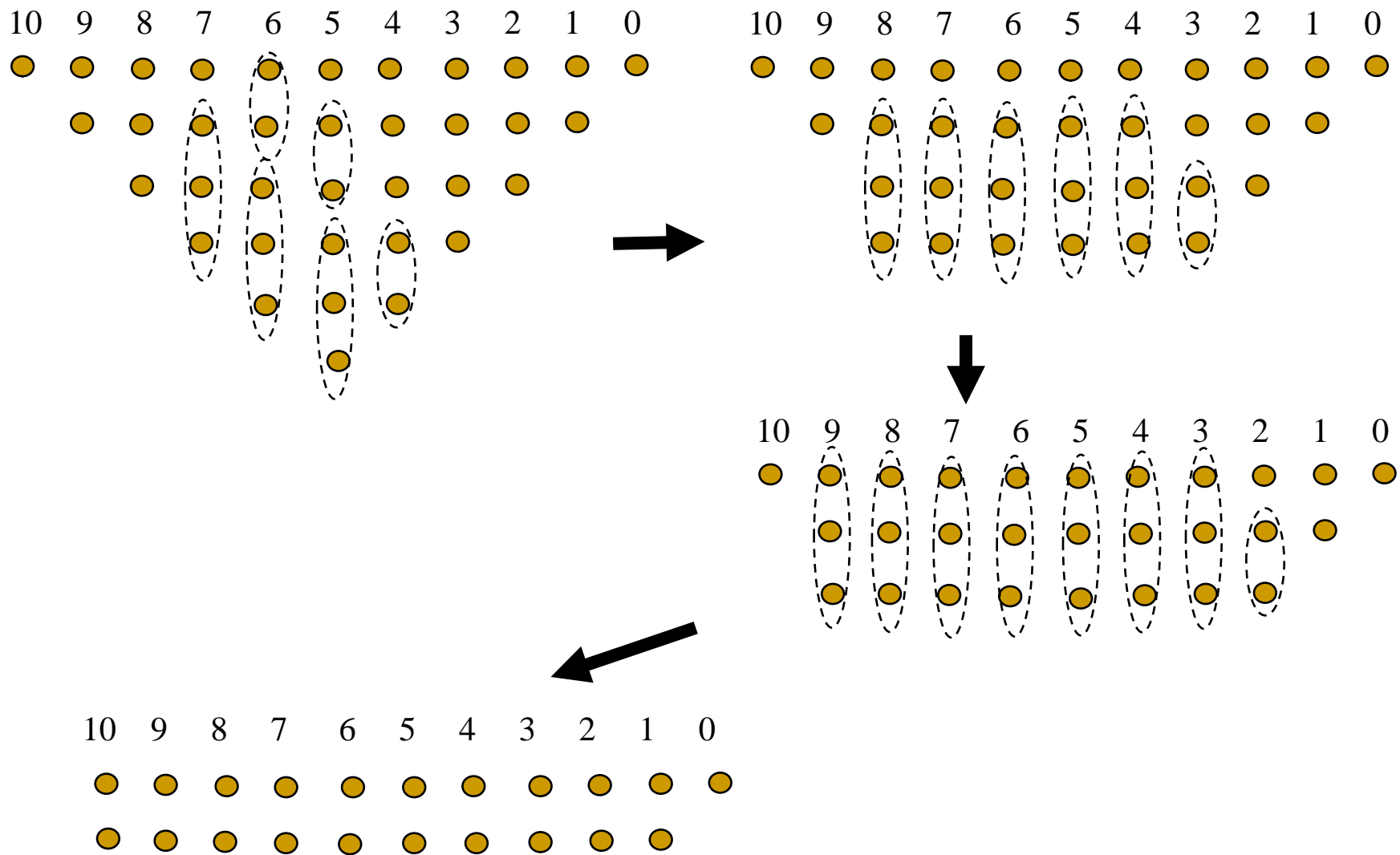


Parallel multiplier

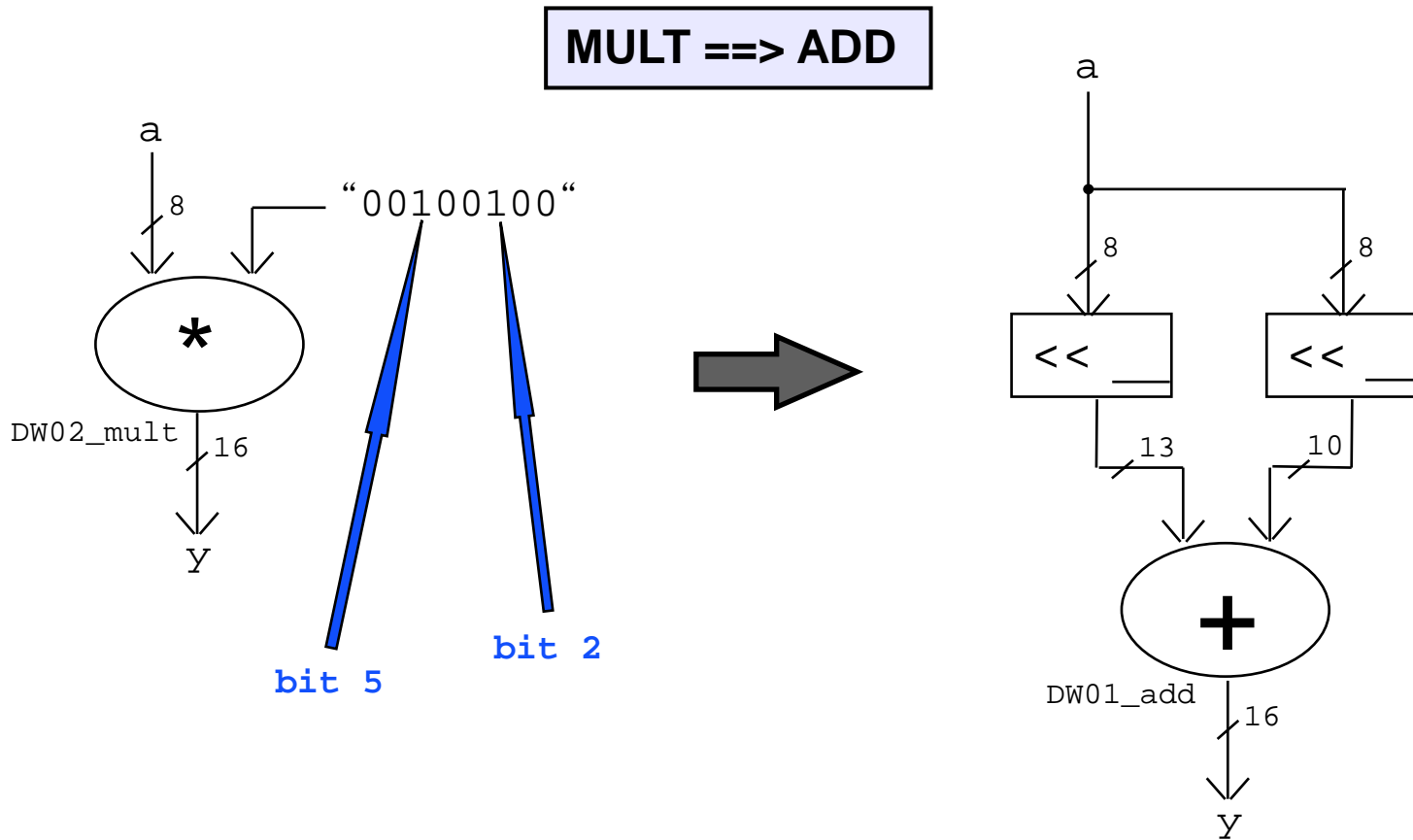
# Reduction of the six partial products (Wallace)



# Reduction of the six partial products (Dadda)



# Constant Multiplication

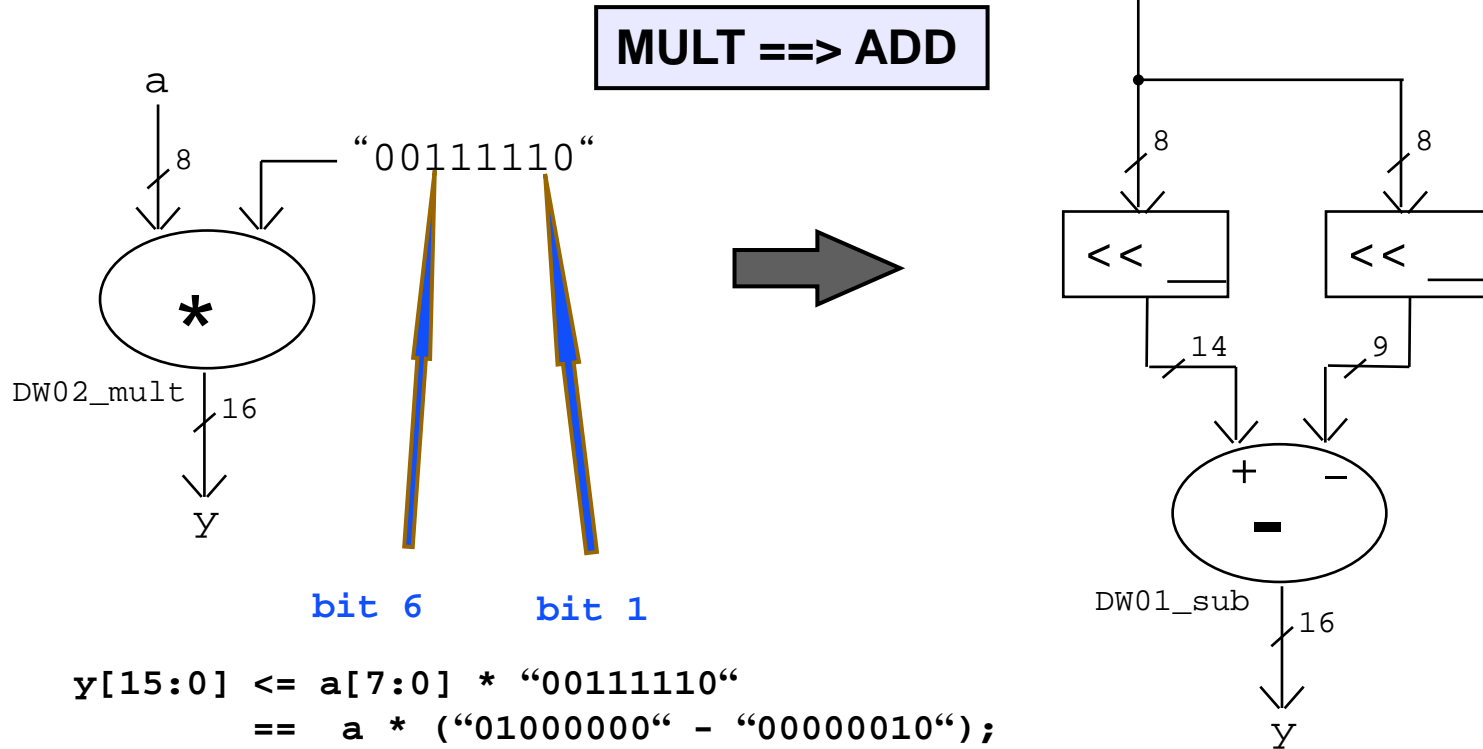


$$\begin{aligned} y[15:0] &\leq a[7:0] * \text{"00100100"} \\ &== (a[7:0] \ll 5) + (a[7:0] \ll 2) \end{aligned}$$

**Constant multiplication by shift-and-add**

# Canonical Encoding

Canonical encoding transforms a constant [vector] such that it contains less '1's than '0's.



**Canonical Encoding for constant multiplication**